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EXAMINER	
WITKOWSKI, ALEXANDER C	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/577,431	CONTA ET AL.	
	Examiner	Art Unit	
	ALEXANDER C. WITKOWSKI	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 - 7, 11 - 21, and 23 - 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Miki et al. (US 6,554,408).

Regarding claim 1, as amended, Miki et al. (US 6,554,408) teaches **an ink** jet printhead (col.1, lines 12-13) comprising one or more ejection modules (Fig.1; col.4, line 14), each including

a silicon chip (Fig.1: 17),

a plurality of ejection nozzles (col.5, lines 61-62) arranged adjacent to an edge of the module (Fig.1: 14, 15, 17),

ejection cells (Fig.1: 12) for said nozzles,

delivery channels (Fig.1: 13) for the ink of the cells, a distribution channel (Fig.1: 13; showing ink channel [distribution channel section] 13 to be the combination of non-tapered and tapered channels in dashed phantom lines with two changes in wall direction between ink inlet 16 and pressure chamber 12) adjacent to the front (Fig.1: showing non-tapered section of distribution channel beginning at ink inlet [front] 16),

each distribution channel (Fig.1: 13) **having a first edge** in fluid communication with the delivery channels (Fig.1: showing external edge [first edge] in dashed phantom lines of connection between a tapered section of ink channel [distribution channel section] 13 and the non-tapered section between the tapered section and the pressure chamber 12) and a **second edge opposite the first edge** (Fig.1: showing internal edge [second edge] in dashed phantom lines on connection between an ink channel [distribution channel section] 13 and the non-tapered section between tapered section of the ink channel [distribution channel section] having an internal edge [second edge] opposite the external edge [first edge] of the ink channel 13), and

a nozzle layer (Fig.1: 18) integrated with the relative chip (Fig.1: 17) and in which **the** ejection nozzles are made parallel to the front (Fig.1: 19);

a support for mounting the module or the modules (Fig.1: 18) and which defines a feeding duct (Fig.1: showing ink inlet [feeding duct] 16) for the ink in fluid communication with said delivery channels (Fig.1: showing ink in fluid communication with non-tapered section [delivery channel section] 13 in dashed phantom lines of connection between a tapered section of ink channel [distribution channel section] 13 and the pressure chamber 12);

a seal between the module or the modules and said support **arranged to form** a fluid seal between the feeding duct of the support and the ejection cells of the module or of the modules (col.2, lines 48-54); **and**

a plurality of ribs (Fig.1: showing ink channel [Examiner considers Miki et al's ink channels to be composed of discrete sections equivalent to Applicants' delivery and distribution channels] 13 separated by ribs {see dashed phantom lines identifying delivery and distribution channels by side wall edges} etched between ink channels [Applicants' delivery and distribution channels] 13) **located in each distribution channel between one or more delivery channels** (Fig.1: showing ribs are located in each ink channel [distribution channel section] 13 between ink channel [delivery channel section] 13)**, the ribs extending transversely across the distribution channel from the first edge to the second edge** (Fig.1: showing ribs extending transversely across ink channel [distribution channel section] 13 from external edge in dashed phantom lines of connection between a tapered section of ink channel [distribution channel section] 13 and the non-tapered section between the tapered section and the pressure chamber 12 [first edge] to an internal edge [second edge] of the ink channel 13)**, and bearing against the nozzle layer** (Fig.1: showing ribs bearing against glass substrate [nozzle layer] 18)**;**

wherein there is one pair of ribs for each delivery channel or one pair of ribs for a plurality of delivery channels (Fig.1: showing a pair of ribs for each ink channel [delivery channel section] 13).

Regarding claim 3, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim 1, characterized in that said distribution channel (Fig.1: showing ink channel [delivery channel section] 13) is defined by a surface etching in the relative silicon chip

(Fig.3E: 35; col.7, lines 18-19).

Regarding claim 4, as amended, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim 1, wherein each chip (Fig.1: 17) defines a reference surface (Fig.1: 18) upon which are arranged **said ejection** cells (Fig.1: 12), **and** the distribution channel of the module or of the modules (Fig.1: 13) is made in an area of a reference surface that includes said front (Fig.1: showing the surface common to elastic body 20 and first silicon substrate 17 [reference surface] that includes left side [front] of 16);

said **seal includes** a sealing lamina having an edge adjacent to the nozzles (Fig.1: 14, 15; Fig.5B: 53, 54, 57) and mounted to provide fluid sealing between the nozzle layer and said support and to cover the feeding duct (col.2, lines 48-54) (Fig.3E: 33; Fig.5B: 52, 57).

Regarding claim 5, as amended, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim **1**, characterized in that said ribs are set adjacent to each delivery channel (Fig.1: showing ribs between each ink channel [delivery channel section] 13).

Regarding claim 6, as amended, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim **1**, characterized in that said ribs are set adjacent to a plurality of delivery channels (Fig.1: showing ribs adjacent to ink channels [delivery channel section] 13).

Regarding claim 7, as amended, Miki et al. teaches a **printhead** (col.1, lines 12-13), as applied to claim **1**, characterized in that the nozzle layer (Fig.1: 18) defines the ejection cells (Fig.1: 12) and the delivery channels (Fig.1: 13) and is fastened to **said** ribs (Fig.1: showing ribs between each ink channel [delivery channel section] 13).

Regarding claim 11, as amended, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim 1, wherein the cells (Fig.1: 12) and the delivery channels (Fig.1: 13) rest upon a given surface of said chip (Fig.1: 17), said head being characterized in that, in said module or in each module, the distribution channel (Fig.1: 13) is made on a surface of the chip opposite said given surface, facing the feeding duct (Fig.1: 16; ink inlet 16) of the mounting support and wherein ducts or slots are provided, passing through said chip which provide fluid connection between the distribution channel on said opposite face and the delivery channels on said given surface (Fig.11: showing ducts or slots pass through the chip in fluid connection between the ink channel [distribution channel section] 13 on opposite face and the ink channel [delivery channel section] 13 on given surface).

Regarding claim 12, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim 11, characterized in that said nozzle layer (Fig.1: 18) acts as a fluid seal for said cells (Fig.1: 12) and for said channels (Fig.1: 13) with respect to said given surface of the chip (col.2: lines 48-52).

Regarding claim 13, Miki et al. teaches a printhead (col.1, lines 12-13) according to claim 11, characterized in that said distribution channel (Fig.1: 13) is adjacent to said front (Fig.1), has no bank and defines in the chip (Fig.1: 17) a projecting section of lesser thickness and in which said nozzle layer (Fig.1: 18) extends over said projecting section (col.4, lines 29-37).

Regarding claim 14, as amended, Miki et al. teaches a printhead (col.1, lines 12-13) according to claim 11, characterized in that said **seal** include**s** sealing material inserted between the nozzle layer (Fig.1: 18) and / or the chip (Fig.1: 17) and said support (Fig.1: 18) (col.2: lines 48-52).

Regarding claim 15, Miki et al. does not teach that said nozzle layer defines spaces above the substrate for a height of 10 - 25 micrometer in said cells and in said delivery channels. It would have been an obvious design choice to one of ordinary skill in the art at the time that this invention was made for the nozzle layer to define spaces above the substrate for a height of 10 - 25 micrometer in cells and in delivery channels in order to more effectively utilize the surface and thickness of the chip.

Regarding claim 16, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim 1, characterized in that it may be used in a parallel or serial-parallel type printing device and comprises a plurality of modules (Fig.1; see col.4, line 14)

aligned along said front (Fig.1) and in which said support (Fig.1: 18) comprises a board of rigid material that defines said feeding duct (Fig.1: 16) through its thickness; and in which said modules are mounted side by side on said board (col.4, lines 28-37: describing Fig.1 as illustrating a plurality of ejection modules) and with the nozzles (Fig.1: 14, 15) aligned parallel (Fig.1) to the front.

Regarding claim 17, as amended, Miki et al. teaches a printhead (col.1, lines 12-13), as applied to claim 16, characterized in that it includes a frame (Fig.1: 18) mounted on said board beside said ejector modules (Fig.1; see col.4, line 14), having the upper surface adjacent to the upper surface of the nozzle layers (Fig.1: 19) of the modules.

Regarding claim 18, as amended, Miki et al. teaches a printhead (col.1, lines 12-13) according to claim 4, characterized in that the upper surface of the frame (Fig.1: 18) is substantially flush with the upper surface of the nozzle layers (Fig.1: 19) and wherein said sealing lamina is mounted tight on the frame and on the nozzle layers of the modules (col.2: lines 48-52), in correspondence with the ribs (Fig.1: 13: showing ribs between each ink channel).

Regarding claim 19, Miki et al. teaches a printhead (col.1, lines 12-13) according to claim 11, characterized in that said sealing material is arranged between said frame (Fig.1: 18) and the nozzle layer (Fig.1: 19) or the relative chip of the modules (Fig.1: 17) (col.2: lines 48-52).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. (US 6,554,408), as applied to claim 1 above.

Regarding claim 2, Miki et al. does not teach that, in said module or in each module the ejection cells are positioned at 0.5 - 1.0 mm from said front. However, it would have been an obvious to one of ordinary skill in the art at the time that this invention was made for the ejection cells in the module or in each module to have been positioned at 0.5 - 1.0 mm from the front, because it would have been an obvious choice of design and recognizable by one of ordinary skill in the art in order to more effectively utilize the surface and thickness of the chip. See MPEP 2144.

Regarding claim 9, as amended, Miki et al. does not teach that the distribution channel is of width 0.3 - 1.0 mm and said ribs extend for a distance of 0.2 - 1.0 mm in said distribution channel. However, it would have been an obvious design choice to one of ordinary skill in the art at the time that this invention was made to make the

distribution channel of width 0.3 - 1.0 mm and the ribs to extend for a distance of 0.2 - 1.0 mm in the distribution channel because it would have been an obvious choice of design and recognizable by one of ordinary skill in the art in order to more effectively utilize the surface and thickness of the chip. See MPEP 2144.

Regarding claim 10, Miki et al. does not teach that said ribs are of width 15-30 micrometers. However, it would have been to one of ordinary skill in the art at the time that this invention was made to make the ribs of width 15-30 micrometers because it would have been an obvious choice of design and recognizable by one of ordinary skill in the art in order to more effectively utilize the surface and thickness of the chip. See MPEP 2144.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. (US 6,554,408), as applied to claim 4 above, in view of Bartky et al. (US 4,879,568).

Regarding claim 8, as amended, Miki et al. does not teach that the sealing lamina is limited by a tapering edge adjacent to said nozzles.

Bartley et al. teaches the sealing lamina is limited by a tapering edge adjacent to said nozzles (col.9, lines 60-63).

It would have been obvious to one of ordinary skill in the art at the time of this invention to modify Miki et al. to provide a sealing lamina on one side of a channel that

is limited by a tapering edge adjacent to the nozzles, as taught by Bartky et al., for the purpose of improving bonding on the tapered side of the channel.

5. Claims 20, 21, 23 - 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miki et al. (US 6,554,408) in view of Tom et al. (US 6,347,861).

Regarding claim 20, as amended, Miki et al. teaches a process for manufacturing an ink jet printhead (col.1, lines 12-13), comprising the step**s** of**;**

preparing ejector modules (Fig.1; col.4, line 14), each including**:**

a chip substrate (Fig.1: 17) with a relative front having a plurality of resistors,

ejection cells (col.5, lines 61-62) and delivery channels (Fig.1: 13) for the ink of the cells,

a distribution channel (Fig.1: 13) **having a first edge** in fluid communication with the delivery channels (Fig.1: showing external edge [first edge] in dashed phantom lines of connection between a tapered section of ink channel [distribution channel section] 13 and the non-tapered section between the tapered section and the pressure chamber 12) and a **second edge opposite the first edge** (Fig.1: showing internal edge [second edge] in dashed phantom lines on connection between an ink channel [distribution channel section] 13 and the non-tapered section between tapered section of the ink channel [distribution channel section] having an internal edge [second edge] opposite the external edge [first edge] of the ink channel 13)**,** and

a nozzle layer (Fig.1: 19) having ejection nozzles (col.5, lines 61-62) aligned with said front and arranged above the resistors and in which the head includes a support (Fig.1: 18) having an ink feeding duct (Fig.1: 16) for one or more modules;

wherein assembling the **ink jet print**head **comprises**:

mounting the module or modules on said support so as to have the distribution channel (Fig.1: 13) or channels in fluid communication with said feeding duct (col.2, lines 48-54);

hydraulically sealing the nozzle layer of the module or of the modules from said support, for ink-tightness in feeding the ink between the feeding duct and the nozzles through said delivery channels (col.2, lines 48-52)**;**

making an etching on a given face of the chip to produce said distribution channel between the front and an area adjacent to the resistors and parallel to the front (Fig.3C; see col.7, lines 5-11: disclosing etching of the ink channel [distribution channel section] 33)**;**

producing sacrificial volumes for defining the limits of the ejection cells above the resistors and the delivery channels above the area (Fig.3D; see col.7, lines 18-19: disclosing etching [producing sacrificial volumes] to form pressure chamber [ejection cell] 34 and ink inlet [delivery channel section] 35)**;**

applying a structural layer over said sacrificial volumes to define said nozzle layer (Figs.5A,B; see col.8, lines 15-21: disclosing bonding [applying structural layer over sacrificial volumes] silicon 58 and glass substrates to form through-hole [nozzle layer] 54)**;**

wherein said etching step produces on said face, in addition to the distribution channel, a series of ribs that extend transversely across the distribution channel from first edge to the second edge, and in which a part of the sacrificial volumes extend into the space between said ribs and on said distribution channel (Fig.3D; see col.7, lines 18-19: disclosing etching [producing sacrificial volumes] ink inlet [distribution channel section] 35 which includes first and second edges)**.**

However, Miki et al. does not teach that **a part of the structural layer is applied on the ribs and remains fastened on said ribs after removal of the sacrificial volumes**.

Tom et al. teaches that **a part of the structural layer is applied on the ribs and remains fastened on said ribs after removal of the sacrificial volumes** (col.27, line 51 to col.28, line 14: disclosing upper structural layer attached before barriers [ribs] are etched).

It would have been obvious to one of ordinary skill in the art at the time of this invention to modify the invention of Miki et al. with the invention of Tom et al. to provide that **a part of the structural layer is applied on the ribs and remains fastened on said ribs after removal of the sacrificial volumes**, as taught in Tom et al., for the purpose of eliminating a process step requiring adhesion of layers subsequent to etching channels, thus improving manufacturing economy.

Regarding claim 21, as amended, the combination of Miki et al. and Tom et al. references teaches a process, as applied to claim 20 above, **further comprising:**

producing the ejection nozzles (Miki et al.: col.5, lines 61-62) on said structural layer in correspondence with the sacrificial volumes of the cells.

Regarding claim 23, as amended, the combination of Miki et al. and Tom et al. references teaches a process, as applied to claim **20**, characterized in that producing **the** sacrificial volumes (Miki et al.: Figs.3A-3E) **comprises**:

(a) covering said distribution channel (Fig.1: 13) with sacrificial photoresist, flush with said data face of the chip;

(b) planarizing the photoresist covering the channel and cleaning the parts adjacent to said distribution channel;

(c) applying a layer of controlled thickness of sacrificial photoresist on said substrate above the resistors (Fig.1: 21), the ribs (Fig.1: showing ribs between each ink channel) and the photoresist covering the channel;

(d) exposing with a mask said layer of controlled thickness for defining said cells, the delivery channels (Fig.1: 13) and the distribution channel and delimiting said ribs (Fig.3D; see col.7, lines 18-19: disclosing etching [producing sacrificial volumes] ink inlet [distribution channel section] 35 which includes etching [delimiting] ribs); and

(e) developing said layer of controlled thickness constituting the sacrificial volumes for said cells, for the delivery channels and for the distribution channel and leaving zones for attachment of the chip beside said cells and the distribution channels

and on said ribs (Fig.3D; see col.7, lines 18-19: disclosing etching [producing sacrificial volumes] ink inlet [distribution channel section] 35).

Regarding claim 24, as amended, the combination of Miki et al. and Tom et al. references teaches a process, as applied to claim 20, characterized in that said longitudinal etching is made on the face of the chip, opposite the said given face, forming a projecting section delimited by said front and in which a slot forming step is provided, in which slots are produced in the thickness of the projecting sections and in correspondence with the delivery channels (Miki et al.: Fig.1: 13) and in which, for assembling of the head, the modules are mounted on the bearing surface of the support (Fig.1: 18) with said slots in fluid connection with the feeding duct of the support.

Regarding claim 25, as amended, the combination of Miki et al. and Tom et al. references teaches a process for manufacturing a **print**head according to claim 20, characterized in that said support (Miki et al.: Fig.1: 18) includes a board with a bearing surface for said chips (Fig.1: 17) and an upper surface adjacent to the feeding duct and a distance from said bearing surface and wherein said upper surface is defined by a frame or is obtained directly from the board, the sealing step including the insertion of **a seal** between the chip or the structural layer and said upper surface (col.2, lines 48-54).

Regarding claim 26, as amended, the combination of Miki et al. and Tom et al. references teaches a process, as applied to claim 22, characterized in that said **seal**

includes a sealing lamina glued between said upper surface and the structural layer, in contrast with said ribs (Miki et al.: col.2, lines 48-54).

Regarding claim 27, as amended, the combination of Miki et al. and Tom et al. references teaches a process according to claim 24, characterized in that said **seal** includes sealing material inserted between the fronts of the chips (Fig.1: 17) and said upper surface (Miki et al.: col.2, lines 48-54).

Response to Arguments

6. Applicants' arguments with respect to claims 1 - 21 and 23 - 27 have been considered but are moot in view of the new grounds of rejection.

Conclusion

7. Applicants' amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEXANDER C. WITKOWSKI whose telephone number is (571) 270-3795. The examiner can normally be reached on Monday - Friday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen D. Meier can be reached on 571-272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A.C.W./

/Stephen D Meier/

Supervisory Patent Examiner, Art Unit 2853